Atmel AVR Microcontroller Family - Product Selection Guide

DEVICE	90S1200	90S2313	90S2343	90S4414	90S8515	90S2333	90S8535	MEGA603	MEGA103
ON-CHIP MEMORY									
FLASH (Bytes)	1K	2K	2K	4K	8K	2K	8K	64K	128K
EEPROM (Bytes)	64	128	128	256	512	128	512	2K	4K
SRAM (Bytes)	0	128	128	256	512	128	512	4K	4K
In-System Programmable (ISP)	YES	YES	YES	YES	YES	YES	YES	YES	YES
HARDWARE FEATURES									
I/O Pins	15	15	5	32	32	20	32	32I/O, 8O, 8I	32I/O, 8O, 8I
On-chip RC Oscillator	YES	NO	YES	NO	NO	NO	NO	NO	NO
Real Time Clock (RTC)	NO	NO	NO	NO	NO	NO	NO	YES	YES
SPI Port	NO	NO	NO	YES	YES	YES	YES	YES	YES
Full Duplex Serial UART	NO	YES	NO	YES	YES	YES	YES	1	1
Watchdog Timer	YES	YES	YES	YES	YES	YES	YES	YES	YES
Timer/Counters	1	2	2	2	2	2	2	3	3
PWM Channels (10-bit)	-	1	-	2	2	1	TBA	2	2
Analogue Comparator	YES	YES	NO	NO	NO	NO	NO	NO	NO
ADC	NO	NO	NO	NO	NO	6CH/10BIT	8CH/10BIT	8CH/10BIT	8CH/10BIT
IDLE and Power Down modes	YES	YES	YES	YES	YES	YES	YES	YES	YES
Interrupts	4	11	3	13	13	14	17	24	24
MISCELLANEOUS									
AVR Instructions	89	118	118	118	118	118	120	121	121
Max External Clock Frequency	12MHz	10MHz	10MHz	8MHz	8MHz	8MHz	8MHz	6MHz	6MHz
Vcc Voltage Range (V)	4.0-6.0V	4.0-6.0V	4.0-6.0V	4.0-6.0V	4.0-6.0V	4.0-6.0V	4.0-6.0V	4.0-6.0V	4.0-6.0V

** Max speed depends on Vcc voltage. Frequencies and Currents listed are for Vcc = 5.0V & T = 25°C*

Please verify correct part codes for low voltage parts before ordering.

Key

SRAM - Static RAM
ISP - In-System Programmable
I/O - Input/Output
ADC - Analogue to Digital Convertor
SPI - Serial Peripheral Interface
PWM - Pulse Width Modulation
PAR - Parallel programming mode
FLASH - Reprogrammable Code Memory
EEPROM - Parallel programming mode

EQUINOX SUPPORT TOOLS										Farnell Order Code	Equinox Order Code
AVR Starter System	ISP/PAR	ISP/PAR	ISP/PAR	ISP/PAR	ISP/PAR	ISP/PAR	ISP only	ACT-UPG1	ACT-UPG1	111-806	EQ-8051-ST1 (UK)
AVR Development System	ZIF-ISP	ZIF-ISP	ZIF-ISP	ZIF-ISP	ZIF-ISP	ZIF-ISP	ZIF-ISP	UISP-UPG1	UISP-UPG1	302-2249	AVR-DV1 (UK)
Micro-ISP Series IV Programmer	ISP only	ISP only	ISP only	ISP only	ISP only	ISP only	ISP only	ISP only	ISP only	302-2286	UISP-S4
Micro-ISP Series IV LV Prog.	ISP only	ISP only	ISP only	ISP only	ISP only	ISP only	ISP only	ISP only	ISP only	302-2298	UISP-LV4
Micro-Pro Device Programmer	PAR only	PAR only	-	ZIF-ISP	ZIF-ISP	-	-	-	-	111-715	MPW-PLUS (UK)
AllWriter Universal Programmer	PAR	PAR	-	PAR	PAR	-	-	-	-	302-2225	SG-ALLWRITER
AVR BASIC LITE	YES (1K)	-	-	-	-	-	-	-	-	111-788	AVR-BAS-LIT
AVR BASIC FULL	YES	YES	YES	YES	YES	YES	YES	YES	YES	302-2330	AVR-BAS-FULL
AT90S8515 Socket Stealer (DIL-40)	NO	NO	NO	YES	YES	NO	NO	NO	NO	302-2365	SS-90S8515-P

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The Embedded Solutions Company

Atmel AVR Microcontroller Family - Product Selection Guide

Continued....

Device	90S1200	90S2313	90S2343	90S4414	90S8515	90S2333	90S8535	MEGA603	MEGA103	Farnell Order Code	Equinox Order Code
EQUINOX SUPPORT TOOLS											
AT90S8515 Socket Stealer (PLCC)	NO	NO	NO	YES	YES	NO	NO	NO	NO	303-1068	SS-90S8515-J
DOBOX-MOD1	YES	YES	YES	YES	YES	NO	YES	NO	NO	121-022	UC-PM1
PACKAGE TYPES (Farnell Codes)											
6AC	-	-	-	-	-	-	-	120-984	120-972		
8JC	-	-	-	111-480	111-508	-	120-959	-	-		
8PC	-	-	-	111-478	111-491	-	120-960	-	-		
10PC	-	111-454	111-430	-	-	-	-	-	-		
10SC	-	111-466	111-442	-	-	-	-	-	-		
12PC	690-752	-	-	-	-	-	-	-	-		
12SC	690-934	-	-	-	-	-	-	-	-		

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Errata

- **Wrong Clearing of XTRF in MCUSR**
- **Reset During EEPROM Write**
- **Verifying EEPROM in System**
- **Serial Programming at Voltages below 3.0 Volts**
- **High I_{CC} in Power Down with External Clock Running**
- **Wrong Latching of RCEN fuse**

6. Wrong Clearing of XTRF in MCUSR

The XTRF flag in MCUSR will be cleared when clearing the PORF-flag. The flag does not get cleared by writing a “0” to it.

Problem Fix/Workaround

Finish the test of both flags before clearing any of them. Clear both flags simultaneously by writing 0 to both PORF and XTRF in MCUCR.

5. Reset During EEPROM Write

If reset is activated during EEPROM write the result is not what should be expected. The EEPROM write cycle completes as normal, but the address registers are reset to 0. The result is that both the address written and address 0 in the EEPROM can be corrupted.

Problem Fix/Workaround

Avoid using address 0 for storage, unless you can guarantee that you will not get a reset during EEPROM write.

4. Verifying EEPROM in System

EEPROM verify in In-System Programming mode cannot operate with maximum clock frequency. This is independent of the SPI clock frequency.

Problem Fix/Workaround

Reduce the clock speed, or avoid using the EEPROM verify feature.

3. Serial Programming av Voltages below 3.0 Volts

At voltages below 3.0 Volts, serial programming might fail.

Problem Fix/Workaround

Keep VCC at 3.0 Volts or higher during In-System Programming.

2. High ICC in Power Down with External Clock Running

When the external clock is running while the device is in power down, the power consuption will be higher that specified.

Problem Fix/Workaround

Stop the external clock while the device is in power down.

1. Wrong Latching of RCEN fuse

If V_{CC} goes below GND and then up to the operating voltage, the RCEN fuse can be read as unprogrammed even if it is programmed. The result of this is that the device starts looking for a clock signal on the external clock input instead of from the internal RC oscillator, making it look as if it “hangs”.

Problem Fix/Workaround

Avoid that V_{CC} goes below GND.

If the device has started with the RCEN fuse read wrong, it can be restarted in the correct mode by taking V_{CC} up to the operating range, then below 0.5 volts and then up again.

8-Bit AVR® Microcontroller with 2K bytes of In-System Programmable Flash

AT90S/LS2343 Rev. F Errata Sheet

Rev. 1193B–01/99

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1193B–01/99/xM

Features

- Utilizes the AVR ® Enhanced RISC Architecture
- AVR - High Performance and Low Power RISC Architecture
- 118 Powerful Instructions - Most Single Clock Cycle Execution
- 2K Bytes of In-System Programmable Flash
  - SPI Serial Interface for In-System Programming
  - Endurance: 1,000 Write/Erase Cycles
- 128 Bytes of In-System Programmable EEPROM
  - Endurance: 100,000 Write/Erase Cycles
- 128 Bytes Internal RAM
- 32 x 8 General Purpose Working Registers
  - 3 Programmable I/O Lines AT90S/LS2323
  - 5 Programmable I/O Lines AT90S/LS2343
- V_{CC}: 4.0 - 6.0V AT90S2323/AT90S2343
- V_{CC}: 2.7 - 6.0V AT90LS2323/AT90LS2343
- Power-On Reset Circuit
- Speed Grades: 0 - 10 MHz AT90S2323/AT90S2343
- Speed Grades: 0 - 4 MHz AT90LS2323/AT90LS2343
- Up to 10 MIPS Throughput at 10 MHz
- One 8-bit Timer/Counter with Separate Prescaler
- External and Internal Interrupt Sources
- Programmable Watchdog Timer with On-chip Oscillator
- Low Power Idle and Power Down Modes
- Programming Lock for Flash Program and EEPROM Data Security
- Selectable On-chip RC Oscillator
- 8-pin Device

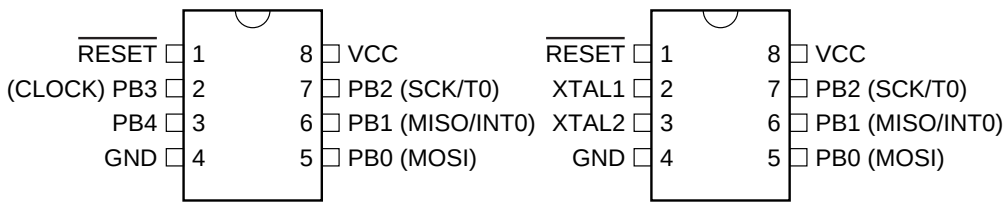
Description

The AT90S/LS2323 and AT90S/LS2343 are low-power CMOS 8-bit microcontrollers based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the AT90S2323/2343 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

Pin Configuration

PDIP/SOIC



AT90S/LS2343 AT90S/LS2323

8-bit AVR® Microcontroller with 2K Bytes of In-System Programmable Flash

AT90S2323
AT90LS2323
AT90S2343
AT90LS2343

Rev. 1004BS–04/99

Note: This is a summary document. For the complete 62 page document, please visit our Website at www.atmel.com or e-mail at literature@atmel.com and request literature #1004C.

Block Diagram

Figure 1. The AT90S/LS2343 Block Diagram

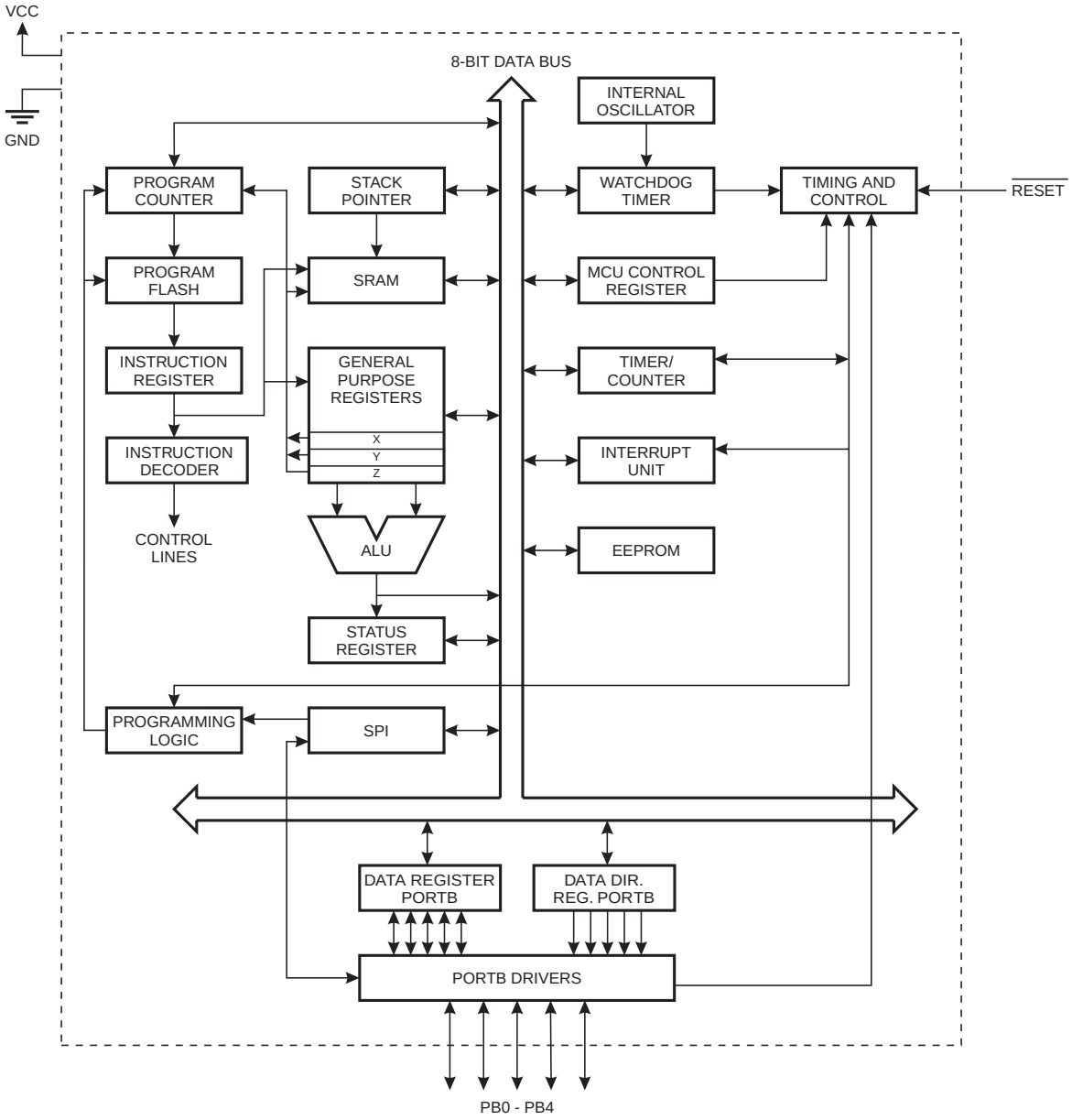
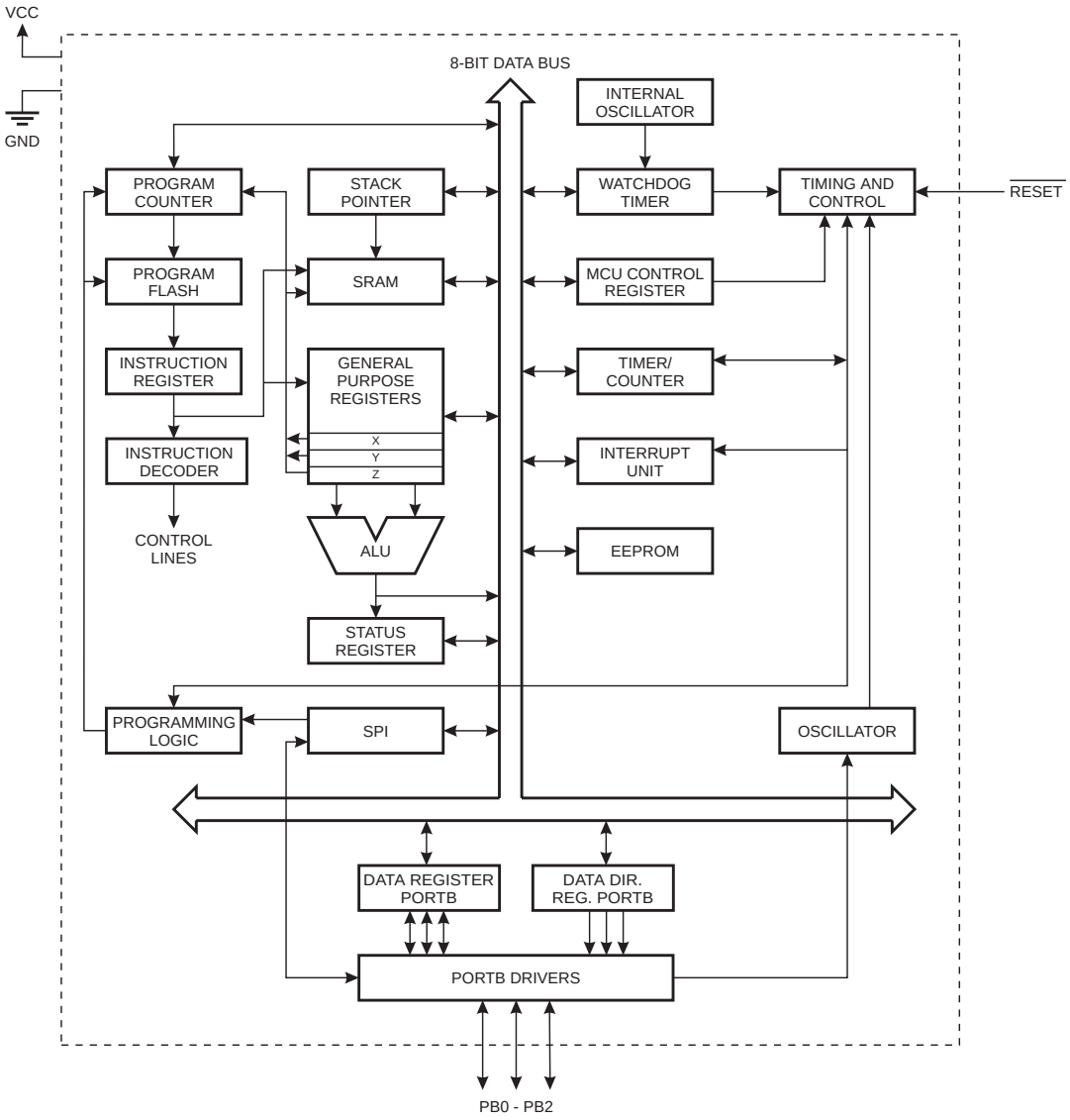


Figure 2. The AT90S/LS2323 Block Diagram



The AT90S2323/2343 provides the following features: 2K bytes of In-System Programmable Flash, 128 bytes EEPROM, 128 bytes SRAM, 3 (AT90S/LS2323)/5 (AT90S/LS2343) general purpose I/O lines, 32 general purpose working registers, an 8-bit timer/counter, internal and external interrupts, programmable Watchdog Timer with internal oscillator, an SPI serial port for Flash Memory downloading and two software selectable power saving modes. The Idle Mode stops the CPU while allowing the SRAM, timer/counters, SPI port and interrupt system to continue functioning. The power down mode saves the register contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.

The device is manufactured using Atmel's high density non-volatile memory technology. The on-chip Flash allows the program memory to be reprogrammed in-system through an SPI serial interface. By combining an 8-bit RISC CPU with ISP Flash on a monolithic chip, the Atmel AT90S2323/2343 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The AT90S2323/2343 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

Comparison Between AT90S/LS2323 and AT90S/LS2343

The AT90S/LS2323 is intended for use with external quartz crystal or ceramic resonator as the clock source. The startup time is fuse selectable as either 1 ms (suitable for ceramic resonator) or 16 ms (suitable for crystal). The device has three I/0 pins.

The AT90S/LS2343 is intended for use with either an external clock source or the internal RC oscillator as clock source. The device has five I/0 pins.

Table 1 summarizes the differences in features of the two devices.

Table 1. Feature Difference Summary

Part	AT90S/LS2323	AT90S/LS2343
On-chip oscillator amplifier	yes	no
Internal RC Clock	no	yes
PB3 available as I/O pin	never	internal clock mode
PB4 available as I/O pin	never	always
Startup time	1 ms / 16 ms	16 µs fixed

Pin Descriptions AT90S/LS2323

V_{CC}

Supply voltage pin.

GND

Ground pin.

Port B (PB2..PB0)

Port B is a 3-bit bi-directional I/O port. Port pins can provide internal pull-up resistors (selected for each bit). The port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

$\overline{\text{RESET}}$

Reset input. An external reset is generated by a low level on the $\overline{\text{RESET}}$ pin. Reset pulses longer than 50 ns will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

Pin Descriptions AT90S/LS2343

V_{CC}
Supply voltage pin.

GND
Ground pin.

Port B (PB4..PB0)
Port B is a 5-bit bi-directional I/O port. Port pins can provide internal pull-up resistors (selected for each bit). When the device is clocked from an external clock source, PB3 is used as the clock input. The port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

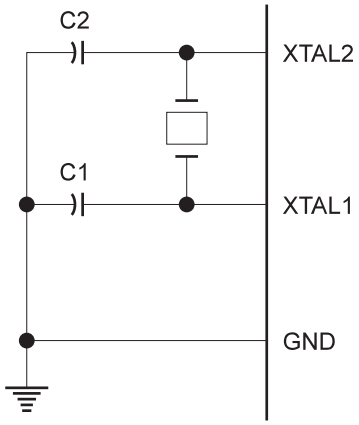
$\overline{\text{RESET}}$
Reset input. An external reset is generated by a low level on the $\overline{\text{RESET}}$ pin. Reset pulses longer than 50 ns will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset.

CLOCK
Clock signal input in external clock mode.

Clock Options

Crystal Oscillator
The AT90S/LS2323 contains an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. XTAL1 and XTAL2 are input and output respectively. Either a quartz crystal or a ceramic resonator may be used. It is recommended to use the AT90S/LS2343 if an external clock source is used, since this gives an extra I/O pin.

Figure 3. Oscillator Connection

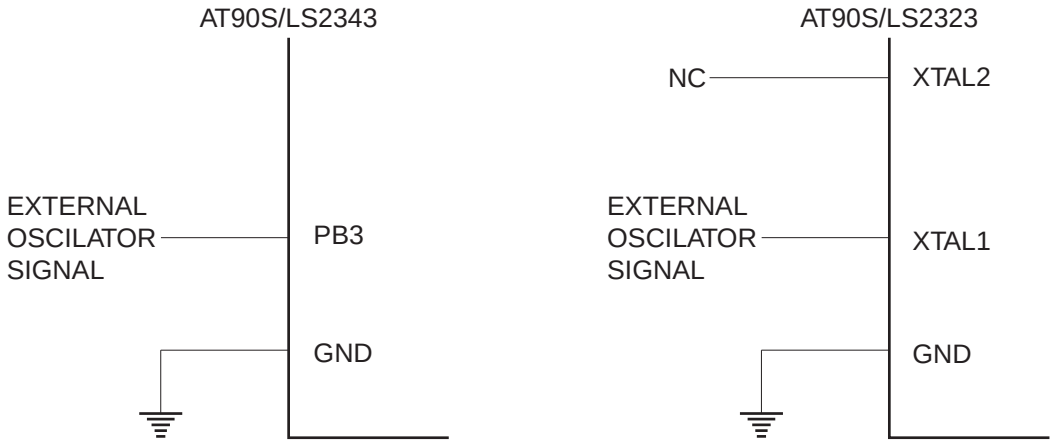


External Clock

The AT90S/LS2343 can be clocked by an external clock signal, as shown in Figure 4, or by the on-chip RC oscillator. This RC oscillator runs at a nominal frequency of 1 MHz (V_{CC} = 5V). A fuse bit - RCEN - in the Flash memory selects the on-chip RC oscillator as the clock source when programmed (“0”). The AT90S/LS2343 is shipped with this bit programmed. The AT90S/LS2343 is recommended if an external clock source is used, because this gives an extra I/O-pin.

The AT90S/LS2323 can be clocked by an external clock as well, as shown in Figure 4. No fuse bit selects the clock source for AT90S/LS2323.

Figure 4. External Clock Drive Configuration

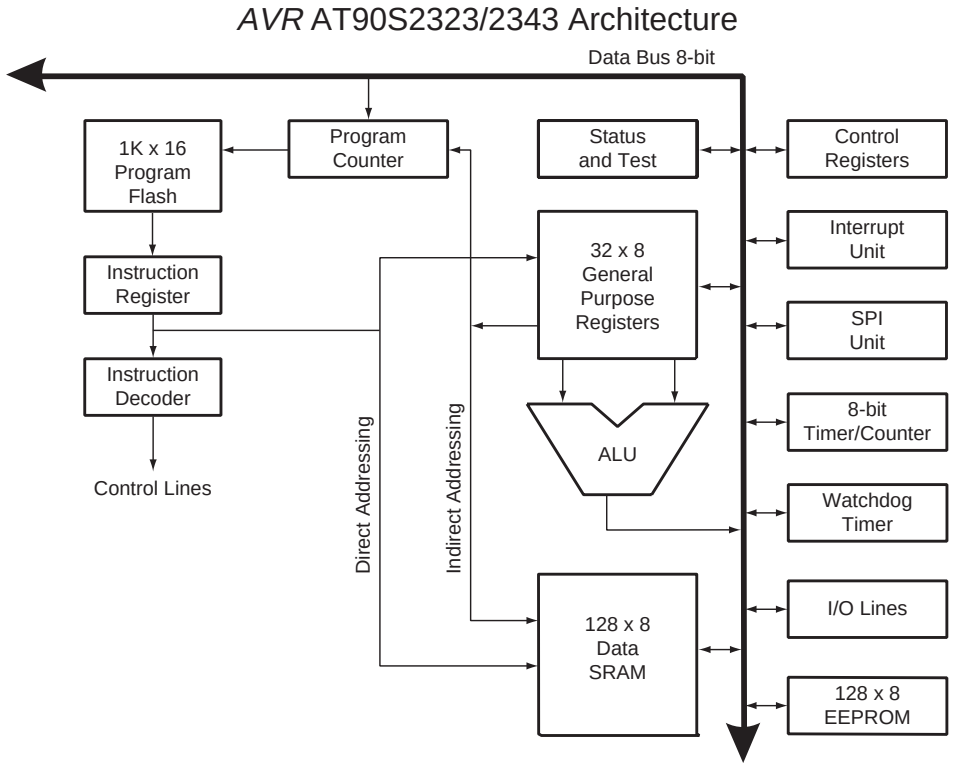


Architectural Overview

The fast-access register file concept contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This means that during one single clock cycle, one ALU (Arithmetic Logic Unit) operation is executed. Two operands are output from the register file, the operation is executed, and the result is stored back in the register file - in one clock cycle.

Six of the 32 registers can be used as three 16-bits indirect address register pointers for Data Space addressing- enabling efficient address calculations. One of the three address pointers is also used as the address pointer for the constant table look up function. These added function registers are the 16-bit X-register, Y-register and Z-register.

Figure 5. The AT90S2323/2343 AVR Enhanced RISC Architecture



The ALU supports arithmetic and logic functions between registers or between a constant and a register. Single register operations are also executed in the ALU. Figure 5 shows the AT90S2323/2343 AVR Enhanced RISC microcontroller architecture.

In addition to the register operation, the conventional memory addressing modes can be used on the register file as well. This is enabled by the fact that the register file is assigned the 32 lowermost Data Space addresses ($00 - $1F), allowing them to be accessed as though they were ordinary memory locations.

The I/O memory space contains 64 addresses for CPU peripheral functions as Control Registers, Timer/Counters, A/D-converters, and other I/O functions. The I/O memory can be accessed directly, or as the Data Space locations following those of the register file, $20 - $5F.

The AVR has Harvard architecture - with separate memories and buses for program and data. The program memory is accessed with a two stage pipeline. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is in-system downloadable Flash memory.

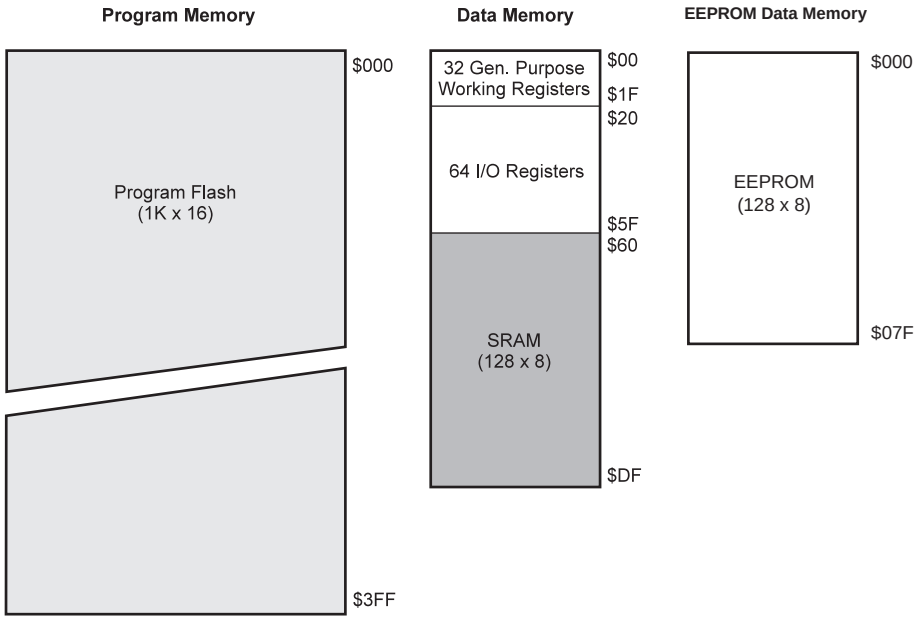
With the relative jump and call instructions, the whole 1K address space is directly accessed. Most AVR instructions have a single 16-bit word format. Every program memory address contains a 16- or 32-bit instruction.

During interrupts and subroutine calls, the return address program counter (PC) is stored on the stack. The stack is effectively allocated in the general data SRAM, and consequently the stack size is only limited by the total SRAM size and the usage of the SRAM. All user programs must initialize the SP in the reset routine (before subroutines or interrupts are executed). The 8-bit stack pointer SP is read/write accessible in the I/O space.

The 128 bytes data SRAM + register file and I/O registers can be easily accessed through the five different addressing modes supported in the AVR architecture.

The memory spaces in the AVR architecture are all linear and regular memory maps.

Figure 6. Memory Maps



A flexible interrupt module has its control registers in the I/O space with an additional global interrupt enable bit in the status register. All the different interrupts have a separate interrupt vector in the interrupt vector table at the beginning of the program memory. The different interrupts have priority in accordance with their interrupt vector position. The lower the interrupt vector address, the higher the priority.

AT90S2323/2343 Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$3F ($5F)	SREG	I	T	H	S	V	N	Z	C
$3E ($5E)	Reserved								
$3D ($5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
$3C ($5C)	Reserved								
$3B ($5B)	GIMSK	-	INT0	-	-	-	-	-	-
$3A ($5A)	GIFR	-	INTF0						
$39 ($59)	TIMSK	-	-	-	-	-	-	TOIE0	-
$38 ($58)	TIFR	-	-	-	-	-	-	TOV0	-
$37 ($57)	Reserved								
$36 ($56)	Reserved								
$35 ($55)	MCUCR	-	-	SE	SM	-	-	ISC01	ISC00
$34 ($54)	MCUSR	-	-	-	-	-	-	EXTRF	PORF
$33 ($53)	TCCR0	-	-	-	-	-	CS02	CS01	CS00
$32 ($52)	TCNT0	Timer/Counter0 (8 Bit)							
$31 ($51)	Reserved								
$30 ($50)	Reserved								
$2F ($4F)	Reserved								
$2E ($4E)	Reserved								
$2D ($4D)	Reserved								
$2C ($4C)	Reserved								
$2B ($4B)	Reserved								
$2A ($4A)	Reserved								
$29 ($49)	Reserved								
$28 ($48)	Reserved								
$27 ($47)	Reserved								
$26 ($46)	Reserved								
$25 ($45)	Reserved								
$24 ($44)	Reserved								
$23 ($43)	Reserved								
$22 ($42)	Reserved								
$21 ($41)	WDTCR	-	-	-	WDTOE	WDE	WDP2	WDP1	WDP0
$20 ($40)	Reserved								
$1F ($3F)	Reserved								
$1E ($3E)	EEAR	-	EEPROM Address Register						
$1D ($3D)	EEDR	EEPROM Data register							
$1C ($3C)	EECR	-	-	-	-	-	EEMWE	EEWE	EERE
$1B ($3B)	Reserved								
$1A ($3A)	Reserved								
$19 ($39)	Reserved								
$18 ($38)	PORTB	-	-	-	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0
$17 ($37)	DDRB	-	-	-	DDB4	DDB3	DDB2	DDB1	DDB0
$16 ($36)	PINB	-	-	-	PINB4	PINB3	PINB2	PINB1	PINB0
$15 ($35)	Reserved								
…	Reserved								
$00 ($20)	Reserved								

Note: 1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

2. Some of the status flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers $00 to $1F only.

Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clock
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	Rd ← Rd + Rr	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	Rd ← Rd + Rr + C	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	Rd ← Rd – Rr	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	Rd ← Rd – K	Z,C,N,V,H	1
SBIW	Rdl,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl – K	Z,C,N,V,S	2
SBC	Rd, Rr	Subtract with Carry two Registers	Rd ← Rd – Rr – C	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	Rd ← Rd – K – C	Z,C,N,V,H	1
AND	Rd, Rr	Logical AND Registers	Rd ← Rd • Rr	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	Rd ← Rd • K	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	Rd ← Rd v Rr	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	Rd ← Rd v K	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	Rd ← Rd ⊕ Rr	Z,N,V	1
COM	Rd	One's Complement	Rd ← $FF – Rd	Z,C,N,V	1
NEG	Rd	Two's Complement	Rd ← $00 – Rd	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • ($FF – K)	Z,N,V	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V	1
DEC	Rd	Decrement	Rd ← Rd – 1	Z,N,V	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V	1
SER	Rd	Set Register	Rd ← $FF	None	1
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC ← Z	None	2
RCALL	k	Relative Subroutine Call	PC ← PC + k + 1	None	3
ICALL		Indirect Call to (Z)	PC ← Z	None	3
RET		Subroutine Return	PC ← STACK	None	4
RETI		Interrupt Return	PC ← STACK	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1 / 2
CP	Rd,Rr	Compare	Rd – Rr	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	Rd – Rr – C	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	Rd – K	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC ← PC + 2 or 3	None	1 / 2
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC ← PC + 2 or 3	None	1 / 2
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC ← PC + 2 or 3	None	1 / 2
SBIS	P, b	Skip if Bit in I/O Register is Set	if (R(b)=1) PC ← PC + 2 or 3	None	1 / 2
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC←PC + k + 1	None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC + k + 1	None	1 / 2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1 / 2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1 / 2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1 / 2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1 / 2
BRLT	k	Branch if Less Than Zero, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1 / 2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1 / 2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1 / 2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1 / 2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1 / 2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1 / 2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1 / 2

Instruction Set Summary (Continued)

Mnemonics	Operands	Description	Operation	Flags	#Clocks
DATA TRANSFER INSTRUCTIONS					
MOV	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	Rd ← (X)	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	Rd ← (X), X ← X + 1	None	2
LD	Rd, - X	Load Indirect and Pre-Dec.	X ← X – 1, Rd ← (X)	None	2
LD	Rd, Y	Load Indirect	Rd ← (Y)	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	Rd ← (Y), Y ← Y + 1	None	2
LD	Rd, - Y	Load Indirect and Pre-Dec.	Y ← Y – 1, Rd ← (Y)	None	2
LDD	Rd,Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	Rd ← (Z), Z ← Z+1	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	Z ← Z - 1, Rd ← (Z)	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2
LDS	Rd, k	Load Direct from SRAM	Rd ← (k)	None	2
ST	X, Rr	Store Indirect	(X) ← Rr	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	(X) ← Rr, X ← X + 1	None	2
ST	- X, Rr	Store Indirect and Pre-Dec.	X ← X - 1, (X) ← Rr	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	(Y) ← Rr, Y ← Y + 1	None	2
ST	- Y, Rr	Store Indirect and Pre-Dec.	Y ← Y - 1, (Y) ← Rr	None	2
STD	Y+q,Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	(Z) ← Rr, Z ← Z + 1	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	Z ← Z - 1, (Z) ← Rr	None	2
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2
STS	k, Rr	Store Direct to SRAM	(k) ← Rr	None	2
LPM		Load Program Memory	R0 ← (Z)	None	3
IN	Rd, P	In Port	Rd ← P	None	1
OUT	P, Rr	Out Port	P ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2
BIT AND BIT-TEST INSTRUCTIONS					
SBI	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
CBI	P,b	Clear Bit in I/O Register	I/O(P,b) ← 0	None	2
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0	Z,C,N,V	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0)←C,Rd(n+1)← Rd(n),C←Rd(7)	Z,C,N,V	1
ROR	Rd	Rotate Right Through Carry	Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0)←Rd(7..4),Rd(7..4)←Rd(3..0)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Twos Complement Overflow	V ← 1	V	1
CLV		Clear Twos Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	3
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1

Ordering Information

Note: The speed grade refers to maximum clock rate when using an external crystal or external clock drive. The internal RC oscillator has the same nominal clock frequency for all speed grades.

Power Supply	Speed (MHz)	Ordering Code	Package	Operation Range
2.7 - 6.0V	4	AT90LS2323-4PC AT90LS2323-4SC	8P3 8S2	Commercial (0°C to 70°C)
		AT90LS2323-4PI AT90LS2323-4SI	8P3 8S2	Industrial (-40°C to 85°C)
4.0 - 6.0V	10	AT90S2323-10PC AT90S2323-10SC	8P3 8S2	Commercial (0°C to 70°C)
		AT90S2323-10PI AT90S2323-10SI	8P3 8S2	Industrial (-40°C to 85°C)
2.7 - 6.0V	4	AT90LS2343-4PC AT90LS2343-4SC	8P3 8S2	Commercial (0°C to 70°C)
		AT90LS2343-4PI AT90LS2343-4SI	8P3 8S2	Industrial (-40°C to 85°C)
4.0 - 6.0V	10	AT90S2343-10PC AT90S2343-10SC	8P3 8S2	Commercial (0°C to 70°C)
		AT90S2343-10PI AT90S2343-10SI	8P3 8S2	Industrial (-40°C to 85°C)

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